What is claimed is:

1. A chip carrier comprising:

a first conductive layer having at least one signal track and at least one contact area, said contact area being electrically connected to said signal track and adapted for transmitting a high-frequency signal; and

a reference structure including a first conductive reference track insulated and spaced from said first conductive layer, said first conductive reference track having a first portion and a second portion spacedly positioned from said first portion, and a second conductive reference track insulated from said first conductive layer and said first conductive reference track, a portion of said second conductive reference track spaced between said first conductive layer and said first conductive reference track, said signal track substantially overlying said portion of said second conductive reference track, and said contact area substantially overlying said first portion of said first conductive reference track, said signal track being electrically shielded by said reference structure.

2. The chip carrier according to claim 1, wherein said at least one contact area includes a solder bump positioned thereon.

3. The chip carrier according to claim 1, wherein said at least one contact area shadows only said first portion of said first conductive reference track.

4. The chip carrier according to claim 1, wherein said first conductive reference track comprises a ground plane.

5. The chip carrier according to claim 1, wherein said second conductive reference track comprises a ground plane.

6. The chip carrier according to claim 1, further including a second conductive layer positioned between said portion of said second conductive reference track and said second portion of said first conductive reference track, said portion of said second conductive reference track including an end surface and said second conductive layer including an end surface, wherein a line drawn between said end surfaces forms an acute angle with said portion of said second conductive reference track.

7. The chip carrier according to claim 6, wherein said second conductive layer comprises a power plane.

8. The chip carrier according to claim 6, wherein said acute angle is about 30° to about 60°.

9. The chip carrier according to claim 8, wherein said acute angle is about 45°.

10. The chip carrier according to claim 6, wherein said portion of said second conductive reference track substantially shadows said second portion of said first conductive reference track and said second conductive layer.

11. The chip carrier according to claim 1, wherein said first conductive layer further includes at least two substantially co-planar electrically conductive tracks, said signal track being positioned between said at least two substantially co-planar electrically conductive tracks, said first conductive layer further including two contact areas other than said at least one contact area, each of said two contact areas electrically coupled to a respective one of said substantially co-planar electrically conductive tracks.

12. The chip carrier according to claim 11, further including a conductive via, said conductive via electrically connecting one of said at least two co-planar tracks to said first portion of said first conductive reference track and to said portion of said second conductive reference track.

13. An electronic package comprising:

a chip carrier including a first conductive layer having at least one signal track and at least one contact area, said

contact area being electrically connected to said signal track and adapted for transmitting a high-frequency signal, said chip carrier further including a reference structure including a first conductive reference track insulated and spaced from said first conductive layer, said first conductive reference track having a first portion and a second portion spacedly positioned from said first portion, and a second conductive reference track insulated from said first conductive layer and said first conductive reference track, a portion of said second conductive reference track spaced between said first conductive layer and said first conductive reference track, said signal track substantially overlying said portion of said second conductive reference track, and said contact area substantially overlying said first portion of said first conductive reference track, said signal track being electrically shielded by said reference structure; and

a semiconductor chip positioned on said chip carrier and having at least one terminal electrically interconnected to said at least one contact area.

14. The chip carrier according to claim 13, wherein said at least one contact area shadows only said first portion of said first conductive reference track.

15. The electronic package of claim 13, further including at least one wire bond, said wire bond electrically coupling said at least one terminal to said at least one contact area.

16. The electronic package of claim 13, wherein said chip carrier further includes a heat sink having a first surface and at least one sidewall therein, said first surface of said heat sink and said side wall defining a cavity within said chip carrier, said semiconductor chip positioned on said surface of said heatsink in said cavity.

17. The electronic package according to claim 13, further including a second conductive layer positioned between said portion of said second conductive reference track and said second portion of said first conductive reference track, said portion of said second conductive reference track including an end surface and said second conductive layer including an end surface, wherein a line drawn between said end surfaces forms an acute angle with said portion of said second conductive reference track.

18. The electronic package according to claim 17, wherein said acute angle is about 30° to about 60°.

19. The electronic package according to claim 18, wherein said acute angle is about 45°.

20. The electronic package according to claim 17, wherein said portion of said second conductive reference track substantially shadows said second portion of said first conductive reference track and said second conductive layer.